REMARKS/ARGUMENTS

The Examiner is thanked for the thorough examination of the present application. Applicant has carefully considered the examiner's opinion and thereby made an amendment to the rejected claims. Claims 1-14 and 16-20 remain in this application and no new matter is entered to any of the remaining claims. Applicant respectfully requests reconsideration for at least the following reasons.

Response to the claim rejections:

Claims 12-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Gersbach et al. (U.S. Patent No. 5,245,637). This rejection is respectfully traversed.

Claim 12 recites:

12. (Currently Amended): A circuit for performing read phase auto-calibration of a storage device, the circuit comprising:

a control unit coupled to the storage device for determining a [[read]]target phase among a plurality of read phases and outputting a multiplexing signal according to the ~~determined read~~ target phase;

a delay chain for generating a plurality of delay signals; and

a multiplexer coupled to the control unit and the delay chain for selecting a delay signal among the delay signals according to the multiplexing signal[[.]];

wherein the control unit reads data stored in the storage device for at least two times according to at least two of the read phases and compares the read data with a predetermined pattern to determine the target phase.

(Emphasis added)

Applicant asserts that the amended claim 12 is patentable over Gersbach because Gersbach at least fails to disclose a combination of the following limitations: "wherein the control unit reads data stored in the storage device for at least two times according to at least two of the read phases and compares the read data with a predetermined pattern to determine the target phase". Gersbach discloses a phase lock logic system 10 for determining (1) the delay or phase shift of a received composite signal with respect to a local clock signal and (2) the difference in frequency between the received signal and local clock signals (Gersbach: Fig. 1; Col. 2, lines 44-49). The system 10 includes a local oscillator 12 which outputs a local clock signal 14 operating at a frequency near that of a received composite clock and data signal 16; a delay element 18 for establishing a plurality of phase-delayed local clock signals ($\Phi 0 \sim \Phi 9$); a data edge sorting circuit 20 for sorting edge transitions in the received composite signal 16 into a number of time intervals corresponding to the number of phase-delayed local clock signals; a series of counters 22 counts the number of these transitions occurring in each of the established time intervals; and **a logic circuit 24 for reading the counters, examining the histogram of the frequency distribution of the counted transitions in the counters**, and determining via the histogram real time changes in the phase and frequency of the received composite signal with respect to the local clock signal. Based on these determinations, the logic circuit 24 issues control signals 32, 34 to enable accurate sampling and reconstruction of the originally transmitted data signal (Gersbach: Fig. 1; Col. 4, lines 27-47). **Gersbach nowhere discloses the logic circuit 24 coupled to a storage device, reading data stored in the storage device for at least two times according to at least two phases and comparing the read data with a predetermined pattern to determine a target phase**. As a result, Gersbach fails to disclose all of the limitations of claim 12 and thereby claim 12 is in condition of allowance. As claims 13-14 are dependent upon claim 12, if claim 12 is found to be allowable, so too should the dependent claims.

Remarks for the newly added claims:

Applicant asserts that the newly added claim 16 is patentable over Gersbach because Gersbach at least fails to disclose a combination of the following limitations: "a control circuit coupled to the storage device for reading given data stored in the storage device according to different read phases, determining a plurality of consecutive phases among the read phases appropriate for correctly reading the given data, and determining a target phase among the consecutive phases and outputting a multiplexing signal according to the target phase". As claims 17-20 are dependent upon claim 16, if claim 16 is found to be allowable, so too should the dependent claims.

Conclusion:

For at least the above-mentioned reasons, all pending claims are submitted to be in condition for allowance. The Examiner is encouraged to telephone the undersigned if there are informalities that can be resolved in a phone conversation, or if the Examiner has any ideas or suggestions for further advancing the prosecution of this case.

Sincerely yours,

/Winston Hsu/ Date: 05.31.2007

Winston Hsu, Patent Agent No. 41,526
P.O. BOX 506, Merrifield, VA 22116, U.S.A.
Voice Mail: 302-729-1562
Facsimile: 806-498-6673
e-mail : winstonhsu@naipo.com

Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)